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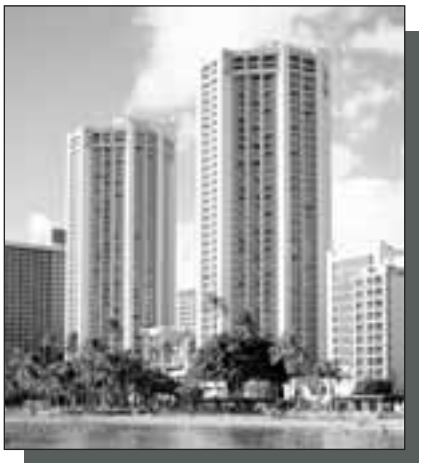
YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at nstojadinovic@elfak.ni.ac.yu

2005 IEEE INTERNATIONAL SOI CONFERENCE (SOI)



Hyatt Regency Waikiki, Honolulu, Hawaii

Hyatt Regency Waikiki - Interior Waterfalls

The 31st Annual IEEE International SOI Conference, the premier conference dedicated to current trends in Silicon-on-Insulator technology, will be held October 3–6, 2005 at the Hyatt Regency Waikiki Resort & Spa in Honolulu, Hawaii. A one-day Tutorial Short Course will precede the conference on Monday, October 2nd.

The SOI conference was established with the support of IEEE to provide a forum for open discussion in all areas of silicon-on-insulator technologies and their applications. Ever increasing demand and modifications in this technology bring the industry together to discuss new accomplishments and gains. Original papers presenting new developments in the industry will be presented at the conference.

The 2005 SOI International Conference will begin with a half-day plenary session followed by two days of oral sessions, a poster session and a late news session. A Best Paper Award will be presented at the closing on Thursday. Session topics will focus on basic materials research, device research, circuit development (special and improved) and applications and uses. Rump sessions will be held on Wednesday evening, October 5. These sessions encourage attendees to share their opinions and expertise on the chosen topics of discussion.

Additionally, a materials and equipment exhibition relating to SOI technology will be held concurrently with the conference. Participants will have the opportunity to visit the exhibit area to see what's new in SOI. Overall, the 2005 SOI International Conference offers attendees a broad spectrum of information, opportunities for discussion with one's peers, and is a must for engineers with direct involvement or partial involvement in SOI.

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nically co-sponsored by EDS will be held in the Hotel Pegaz, Krakow, Poland. The areas of interest are as follows:

- Design of Integrated Circuits and Microsystems
- Thermal Issues in Microelectronics
- Analysis and Modelling of IC and Microsystems
- Microelectronics Technology and Packaging
- Testing and Reliability
- Power Electronics
- Signal Processing
- Embedded Systems
- Medical Applications
- Information Technology
- Education

During the conference there are five special sessions and a tutorial planned:

- "Advanced Compact Modeling and its Standardization Compact Models as Link between R&D, Foundry and IC Design" organised by Dr. Wladyslaw Grabinski, Freescale Geneva, Switzerland and Prof. Hiroshi Iwai, Tokyo Institute of Technology, Japan
- "Special Topics in Emerging Electronics Technologies" organised by Dr. Daniel Foty, Gilgamesh Associates, USA
- "A glimpse into the future" with top speakers from Europe, Japan and the USA (presentations about future directions of microelectronics, nanoelectronics and related technologies).
- CARE Project Special Session organised by Dr. Stefan Simrock and Prof. Dieter Proch
- EDUCHIP Project Special Session coordinated by Prof. Wieslaw Kuzmicz from WUT and Prof. Andrzej Kos from AGH in Krakow

And a tutorial entitled:

- Quality-driven System on Chip Design coordinated by Prof. Lech Jozwiak from Tu/e, The Netherlands.

During the conference, the meeting of the IEEE ED Poland Chapter is planned. All people interested in this meeting, in particular all the members of the Polish section of IEEE, are invited to take part in the event. For more information, please refer to http://www.mixdes.org.

~ Andrzej Napieralski, Editor

ED Benelux

- by Hans Wallinga

Thursday, 27 January 2005, the ED Benelux Chapter organized a colloquium by Prof. Dr. Gijs Bosman of the department of Electrical and Computer Engineering of the University of Florida in Gainesville. His tutorial entitled "Low Frequency Excess Noise and Charge Transport in Carbon Nanotubes", was attended by 42 persons of which approximately 50% were IEEE members.

Professor Bosman started his presentation by explaining the favorable electrical, mechanical, and growth properties of carbon nanotubes. These are the reason that carbon nanotubes moved to the forefront of the research community as serious contenders for leading roles in future nano-scale device technology and circuitry. An important figure of merit for determining their usefulness for electronic applications, especially at the nanoscale, is noise characteristics. After a general introduction to charge transport in these structures the talk focused on their noise characteristics. The shot noise of carbon nanotubes was reported to be suppressed. However, the 1/f noise of carbon nanotubes was found to be unexpectedly high. To delineate the physical mechanisms that contribute to these, potentially show stopping, high noise levels, we measured the noise spectral density at frequencies between 10Hz and 100 kHz over a temperature range from 77K to 300K. The noise observed is a combination of low frequency excess noise and thermal noise. The excess noise spectra showed the presence of Lorentzian noise components superimposed on 1/f noise and were found to be a function of temperature. Using this temperature dependence, the noise producing trap energies, both discrete and distributed, were calculated and interpreted in terms of the carbon nanotube bandstructures.

~ Cora Salm, Editor

ASIA & PACIFIC (REGION 10)

ED Japan

-by Hiroshi Ishiwara

On January 17th, the third Japan Chapter Student Award was given to Hiroyuki Ito (Tokyo Institute of Technology), Hiroshi Irie (University of Tokyo), Takafumi Kamimura (Osaka University), Takeshi Kawano (Toyohashi University of Technology) and Masumi Saitoh

Winners of the 3rd Japan Chapter Student Award and Prof. H. Ishiwara (Chair of EDS Japan Chapter – on the left).

(University of Tokyo). This award was established in 2002 to encourage student members who actively contribute to the research of electron devices. The Japan Chapter selected these five students who have shown outstanding activities in the last year. They received metallic certificate plaques and premium from the Chapter Chair at the Japan Chapter annual meeting held in Tokyo on January 17th.

After the annual meeting, the briefing session for the 2004 IEDM was held to provide a summary discussion on the highlights of the 2004 IEDM. The five invited speakers delivered topics covering Integrated Circuits, CMOS Devices, CMOS Interconnects/Process, Modeling/Simulation, and Compound/Quantum Devices. This session has won popularity with a lot of the Japanese engineers who did not have a chance to attend the last IEDM to discuss the most advanced information of electron device technology. The session was very successful with 100 participants.

The Distinguished Lecturers Meeting was held on February 9th by the Japan Chapter, at Tokyo Institute of Technology in Yokohama, Japan. Two prestigious speakers from EDS gave presentations on: "On the Scaling Issues and High-k Replacement of Ultrathin Gate Dielectrics for Nanoscale MOS Transistors" by Prof. Hei Wong (City University of Hong Kong, China), and "The new generation of the photoelectric measurement methods of the MOS structure parameters" by Prof. Henryk M. Przewlocki (Institute of Electron Technology, Poland.

ED Kansai

- by Toshimasa Matsuoka

The ED Kansai Chapter held a Technical Meeting at Osaka University, Osaka,